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2. **IDAP: a tool for high-level power estimation of custom array structures**
Mamidipaka, M.; Khouri, K.; Dutt, N.; Abadir, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 23, Issue 9, Sept. 2004 Page(s):1361 - 1369
Digital Object Identifier 10.1109/TCAD.2004.833609
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Zarrineh, K.; Upadhyaya, S.J.; Chickermane, V.;
Design & Test of Computers, IEEE
Volume 18, Issue 3, May-June 2001 Page(s):83 - 97
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Tze-Thong Chen; Adams, M.;
Automatic Control, IEEE Transactions on
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4. **Integrating development- and support tools for PHM in Saab 39 Gripen**
Fransson, T.;
Aerospace Conference, 2006 IEEE
4-11 March 2006 Page(s):12 pp.
Digital Object Identifier 10.1109/AERO.2006.1656071
AbstractPlus | Full Text: PDF(1248 KB) IEEE CNF
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5. **Nonlinear Fault Detection and Isolation in a Three-Tank Heating System**
Mattone, R.; De Luca, A.;
Control Systems Technology, IEEE Transactions on
Volume 14, Issue 6, Nov. 2006 Page(s):1158 - 1166
Digital Object Identifier 10.1109/TCST.2006.880221
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6. **Maintainability Simulation and Demonstration Equipment Description and Application**
Buchaca, N.; Brinda, J., Jr.;
Product Engineering and Production, IEEE Transactions on
Volume 7, Issue 1, Jan 1963 Page(s):6 - 12
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7. **IDAP: a tool for high-level power estimation of custom array structures**
Mamidipaka, M.; Khouri, K.; Dutt, N.; Abadir, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 23, Issue 9, Sept. 2004 Page(s):1361 - 1369
Digital Object Identifier 10.1109/TCAD.2004.833609
AbstractPlus | References | Full Text: PDF(488 KB) IEEE JNL
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8. **Sequence-switch coding for low-power data transmission**
Myungchul Yoon;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 12, Issue 12, Dec 2004 Page(s):1381 - 1385
Digital Object Identifier 10.1109/TVLSI.2004.837995
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9. **Design, selection and implementation of a content-addressable memory for a VLSI CMOS ch**
Jones, S.;
Computers and Digital Techniques, IEE Proceedings-
Volume 135, Issue 3, May 1988 Page(s):165 - 172
AbstractPlus | Full Text: PDF(792 KB) IET JNL

10. **Instrument fault detection and compensation scheme for direct torque controlled induction**
Lee, K.-S.; Ryu, J.-S.;
Control Theory and Applications, IEE Proceedings-
Volume 150, Issue 4, 24 July 2003 Page(s):376 - 382
Digital Object Identifier 10.1049/ip-cta:20030596
AbstractPlus | Full Text: PDF(279 KB) IET JNL

11. **Robust fault detection of uncertain linear systems via quasi-LMIs**
Casavola, A.; Famularo, D.; Franze, G.;
American Control Conference, 2005. Proceedings of the 2005
8-10 June 2005 Page(s):1654 - 1659 vol. 3
Digital Object Identifier 10.1109/ACC.2005.1470205
AbstractPlus | Full Text: PDF(403 KB) IEEE CNF
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12. **Embedded DRAM (eDRAM) power-energy estimation for system-on-a-chip (SoC) application**
Yong-Ha Park; Jeonghoon Kook; Hoi-Jun Yoo;
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific International Conference on VLSI Design. Proceedings.
7-11 Jan. 2002 Page(s):625 - 630
Digital Object Identifier 10.1109/ASPDAC.2002.995006
AbstractPlus | Full Text: PDF(321 KB) IEEE CNF
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13. **Methods for fault diagnosis in rail vehicle traction and braking systems**
Daley, S.; Newton, D.A.; Bennett, S.M.; Patton, R.J.;
Qualitative and Quantitative Modelling Methods for Fault Diagnosis, IEE Colloquium on

24 Apr 1995 Page(s):5/1 - 513

AbstractPlus | Full Text: PDF(828 KB) IET CNF

14. **A floating point co-processor for real-time fault detection and isolation in electronically cont**
Yu, T.; Rizzoni, G.;
Automotive Electronics, 1991., Eighth International Conference on
28-31 Oct 1991 Page(s):53 - 57

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1. **A scalable algorithm for RTL insertion of gated clocks based on ODCs computation**
Babighian, P.; Benini, L.; Macii, E.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 24, Issue 1, Jan. 2005 Page(s):29 - 42
Digital Object Identifier 10.1109/TCAD.2004.839489(410) 24
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2. **IDAP: a tool for high-level power estimation of custom array structures**
Mamidipaka, M.; Khouri, K.; Dutt, N.; Abadir, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 23, Issue 9, Sept. 2004 Page(s):1361 - 1369
Digital Object Identifier 10.1109/TCAD.2004.833609
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3. **Design, selection and implementation of a content-addressable memory for a VLSI CMOS ch**
Jones, S.;
Computers and Digital Techniques, IEE Proceedings-
Volume 135, Issue 3, May 1988 Page(s):165 - 172
AbstractPlus | Full Text: PDF(792 KB) IET JNL

4. **A Clock Isolation Method For Complex SoC Designs**
Kaijian Shi; Belhadj, H.;
SOC Conference, 2005. Proceedings. IEEE International
25-28 Sept. 2005 Page(s):251 - 256
Digital Object Identifier 10.1109/SOCC.2005.1554505
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1 Process oriented logic simulation
Sany M. Leinwand
June 1981 **Proceedings of the 18th conference on Design automation DAC '81**
Publisher: IEEE Press
Full text available: pdf(662.44 KB) Additional Information: full citation, abstract, references, index terms

Theoretically, simulation can be activity oriented, event oriented or process oriented. Existing techniques for logic simulation are either activity or event oriented. In this paper, the possibility of logic simulation using process oriented concepts is investigated. Such an approach is justified by the need to support modular design environments. The key feature is that of asynchronous module activity: the timing order of signal changes has to be preserved only for those events belonging t ...

2 Faults: Configurable isolation: building high availability systems with commodity multi-core processors
Nidhi Aggarwal, Parthasarathy Ranganathan, Norman P. Jouppi, James E. Smith
June 2007 **Proceedings of the 34th annual international conference on Computer architecture ISCA '07**
Publisher: ACM Press
Full text available: pdf(458.30 KB) Additional Information: full citation, abstract, references, index terms

High availability is an increasingly important requirement for enterprise systems, often valued more than performance. Systems designed for high availability typically use redundant hardware for error detection and continued uptime in the event of a failure. Chip multiprocessors with an abundance of identical resources like cores, cache and interconnection networks would appear to be ideal building blocks for implementing high availability solutions on chip. However, doing so poses significan ...

Keywords: chip multiprocessors, fault isolation, high availability

3 Parallel logic simulation of VLSI systems
Mary L. Bailey, Jack V. Briner, Roger D. Chamberlain
September 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 3
Publisher: ACM Press
Full text available: pdf(3.74 MB) Additional Information: full citation, abstract, references, citings, index terms

Fast, efficient logic simulators are an essential tool in modern VLSI system design. Logic simulation is used extensively for design verification prior to fabrication, and as VLSI systems grow in size, the execution time required by simulation is becoming more and more significant. Faster logic simulators will have an appreciable economic impact, speeding time to market while ensuring more thorough system design testing. One approach to this problem is to utilize parallel processing, taking ...

Keywords: circuit structure, parallel architecture, parallelism, partitioning, synchronization algorithm, timing granularity

4 Architectural design techniques for high performance and robustness: A new paradigm for low-power, variation-tolerant circuit synthesis using critical path isolation

Swaroop Ghosh, Swarup Bhunia, Kaushik Roy

November 2006 **Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design ICCAD '06**

Publisher: ACM Press

Full text available: pdf(327.06 KB) Additional Information: full citation, abstract, references

Design considerations for robustness with respect to variations and low power operations typically impose contradictory design requirements. Low power design techniques such as voltage scaling, dual-Vth etc. can have a large negative impact on parametric yield. In this paper, we propose a novel paradigm for low-power variationtolerant circuit design, which allows aggressive voltage scaling. The principal idea is to (a) isolate and predict the set of possible paths that may become c ...

5 Functional testing A user looks at logic simulation

William L. Keiner

June 1973 **Proceedings of the 10th workshop on Design automation DAC '73**

Publisher: IEEE Press

Full text available: pdf(572.34 KB) Additional Information: full citation, abstract, references, index terms

This paper attempts to identify the capabilities required to be present in a logic simulation system in order to make it an effective analysis tool for logic design verification and test verification.

6 A methodology for hardware verification based on logic simulation

Randal E. Bryant

April 1991 **Journal of the ACM (JACM)**, Volume 38 Issue 2

Publisher: ACM Press

Full text available: pdf(1.98 MB) Additional Information: full citation, abstract, references, citings, index terms, review

A logic simulator can prove the correctness of a digital circuit if it can be shown that only circuits fulfilling the system specification will produce a particular response to a sequence of simulation commands.This style of verification has advantages over the other proof methods in being readily automated and requiring less attention on the part of the user to the low-level details of the design. It has advantages over other approaches to simulation in providing more reliable results, oft ...

7 TEGAS2—anatomy of a general purpose TEST GENERATION AND SIMULATION system for digital logic

S. A. Szygenda

June 1972 **Proceedings of the 9th workshop on Design automation DAC '72**

Publisher: ACM Press

Additional Information:

Full text available: pdf(1.19 MB) full citation, abstract, references, citings, index terms

This paper will attempt to consider requirements and problems encountered in the development of digital logic simulation and test generation systems. The procedure for doing this will be to first consider requirements and general considerations for a particular simulation system (TEGAS2(1,2)TEST GENERATION AND SIMULATION) and then to dissect the system into its major constituent ...

8 TEGAS2 - Anatomy of a general purpose test generation and simulation system for digital logic

S. A. Szygenda

June 1988 **Papers on Twenty-five years of electronic design automation 25 years of DAC**

Publisher: ACM Press

Full text available: pdf(1.43 MB) Additional Information: full citation, references, index terms

9 SIGDA 2 - Design automation: Modular requirements for digital logic simulation at a predefined functional level

C. W. Hemming, S. A. Szygenda

August 1972 **Proceedings of the ACM annual conference - Volume 1 ACM'72**

Publisher: ACM Press

Full text available: pdf(882.95 KB) Additional Information: full citation, abstract, references, citings

Simulation of digital logic provides a viable technique for development and diagnosis of digital systems. Simulation models currently employed are discussed with a summary of structure and timing techniques. A methodology for functional simulation in conjunction with gate level simulation is discussed, presenting a representative set of predefined functions, and introducing a measure for predefined function performance. Errors in design detectable at the functional level are catagorized.

Keywords: diagnosis of digital systems, digital simulation, fault simulation, functional simulation, logic design

10 Fundamentals of parallel logic simulation

Robert J. Smith

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation DAC '86**

Publisher: IEEE Press

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings, index terms

Parallel processing is being recognized as a practical way to achieve very high performance in logic simulation of large designs. This tutorial summarizes many of the basic methods employed, and estimates attainable throughput. Next, data structuring and processing factors are explored as they impact parallel simulation. Experience indicates that support processing necessary before and after simulation kernel execution can be accelerated using parallel methods. We conclude by suggesting pit ...

11 Logic simulation and fault analysis of a self-checking switching processor

H. Y. Chang, R. C. Dorr, R. A. Elliott

June 1972 **Proceedings of the 9th workshop on Design automation DAC '72**

Publisher: ACM Press

Full text available: Additional Information:

pdf(542.26 KB) full citation, abstract, references, index terms

During an exploratory study in the design of a stored program processor for an electronic switching system, the need for logic simulation for design verification was evident [1]. The advantages of using logic simulation concurrent with hardware design are many. This paper will discuss logic simulation and fault analysis work undertaken while designing a self-checking switching processor. The logic simulation and fault analysis were implemented on an IBM/360 model 67 executing a s ...

12 Logical process size in parallel simulations

Fang Hao, Karen Wilson, Richard Fujimoto, Ellen Zegura
November 1996 **Proceedings of the 28th conference on Winter simulation WSC '96**
Publisher: ACM Press, IEEE Computer Society
Full text available: pdf(852.62 KB) Additional Information: full citation, abstract, references, citings

Most existing synchronization protocols require that the simulation application be partitioned and mapped to logical processes to make it suitable for parallel execution. Assuming the simulation models some number of physical components, an important design question is how many components should be mapped to each logical process? This is a nontrivial question because logical process "size" affects the efficiency of the synchronization protocol, load balance, and approach for implementing shared ...

13 A transistor-level logic-with-timing simulator for MOS circuits

Thomas J. Schaefer
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation DAC '85**
Publisher: ACM Press
Full text available: pdf(501.75 KB) Additional Information: full citation, abstract, references, citings, index terms

VTIsim is a transistor-level simulator for MOS circuits which provides logic simulation together with approximate timing estimates based on layout information. Two novel features enhance the accuracy of simulation: node states are represented as voltages rather than as logic states, and node transitions are modeled as voltage ramps rather than as steps taking place at a fixed instant. This paper describes the major features of the simulator, some issues in its design, and the benefits and p ...

14 Utilizing logic information in multi-level timing simulation

Marko P. Chew, Andrzej J. Strojwas
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation DAC '91**
Publisher: ACM Press
Full text available: pdf(587.30 KB) Additional Information: full citation, references, index terms

15 A hybrid scheduling technique for hierarchical logic simulators or "Close Encounters of the Simulated Kind"

Will Sherwood
June 1979 **Proceedings of the 16th Conference on Design automation DAC '79**
Publisher: IEEE Press
Full text available: pdf(392.02 KB) Additional Information: full citation, abstract, citings, index terms

Advancing circuit complexity in LSI technology has brought about an ever growing need for more powerful Computer Aided Design tools. Verification of an IC design through simulation is mandatory to avoid costly mask iterations and delays in product introduction due to design errors. A gate level simulation is one method for reducing errors in a chip

design. However, gate level simulations of large designs are extremely expensive. A high level "black box" or functional simulation ...

Keywords: Event-driven and fixed event list scheduling techniques, Logic Simulation, RT/Gate level descriptions, Software breadboard

16 Survey of analysis, simulation and modeling for large scale logic circuits

Albert E. Ruehli

June 1981 **Proceedings of the 18th conference on Design automation DAC '81**

Publisher: IEEE Press

Full text available: pdf(481.15 KB) Additional Information: full citation, abstract, references, citings, index terms

The purpose of this paper is to introduce recent developments in the time analysis, simulation and modeling of logic circuits. These advances which have taken place in the circuit and systems area augment the recent advances in logic time simulators. The latest trend has been to combine the approaches into a single system, a so called mixed simulation-analysis program. In this paper we review some of the circuit oriented techniques at a level understandable to the non circuit-theorist.

17 Modular requirements for digital logic simulation at a predefined functional level

C. W. Hemming, S. A. Szygenda

September 1972 **ACM SIGDA Newsletter**, Volume 2 Issue 2-3

Publisher: ACM Press

Full text available: pdf(834.57 KB) Additional Information: full citation, references

18 Fault simulation of digital logic utilizing a small host machine

Robert M. McClure

June 1972 **Proceedings of the 9th workshop on Design automation DAC '72**

Publisher: ACM Press

Full text available: pdf(525.05 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a simulation system for use in the generation of test programs for logic networks. This system was designed and implemented by Telpar, Inc. specifically for use in providing a commercial service for the generation of digital test programs. The simulator described here was originally written in the fall of 1970, and has been in constant use since. There have been more or less continuous improvements, but the basic system has remained unchanged since its original implemen ...

19 Functional simulation and fault diagnosis

Miroslaw Malek, Ajoy K. Bose

June 1978 **Proceedings of the 15th conference on Design automation DAC '78**

Publisher: IEEE Press

Full text available: pdf(570.23 KB) Additional Information: full citation, abstract, references, citings, index terms

Some aspects of the application of functional simulation to fault diagnosis are discussed. A technique for functional simulation that preserves a high level of accuracy is described. Applicability of this method to fault simulation and diagnosis is shown by presenting an approach to diagnostic testing and giving an algorithm for test point placement. The compatibility of the functional simulation technique and the partitioning of the system for diagnosis is indicated.

20 Automating RT-level operand isolation to minimize power consumption in datapaths

M. Münch, B. Wurth, R. Mehra, J. Sproch, N. Wehn

January 2000 **Proceedings of the conference on Design, automation and test in Europe DATE '00**

Publisher: ACM Press

Full text available: pdf(116.10 KB) Publisher Site

Additional Information: full citation, references, citings, index terms

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1 Mondrix: memory isolation for linux using mondriaan memory protection

Emmett Witchel, Junghwan Rhee, Krste Asanović

October 2005 **ACM SIGOPS Operating Systems Review , Proceedings of the twentieth ACM symposium on Operating systems principles SOSP '05**, Volume 39 Issue 5

Publisher: ACM Press

Full text available: pdf(332.09 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the design and an evaluation of Mondrix, a version of the Linux kernel with Mondriaan Memory Protection (MMP). MMP is a combination of hardware and software that provides efficient fine-grained memory protection between multiple protection domains sharing a linear address space. Mondrix uses MMP to enforce isolation between kernel modules which helps detect bugs, limits their damage, and improves kernel robustness and maintainability. During development, MMP exposed two kerne ...

Keywords: fine-grained memory protection

2 Faults: Configurable isolation: building high availability systems with commodity multi-core processors

Nidhi Aggarwal, Parthasarathy Ranganathan, Norman P. Jouppi, James E. Smith

June 2007 **Proceedings of the 34th annual international conference on Computer architecture ISCA '07**

Publisher: ACM Press

Full text available: pdf(458.30 KB) Additional Information: full citation, abstract, references, index terms

High availability is an increasingly important requirement for enterprise systems, often valued more than performance. Systems designed for high availability typically use redundant hardware for error detection and continued uptime in the event of a failure. Chip multiprocessors with an abundance of identical resources like cores, cache and interconnection networks would appear to be ideal building blocks for implementing high availability solutions on chip. However, doing so poses significan ...

Keywords: chip multiprocessors, fault isolation, high availability

3 Achieving extensibility through product-lines and domain-specific languages: a case

study
Don Batory, Clay Johnson, Bob MacDonald, Dale von Heeder
April 2002 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 11 Issue 2
Publisher: ACM Press

Full text available: pdf(324.37 KB) Additional Information: full citation, abstract, references, citings, index terms, review

This is a case study in the use of *product-line architectures (PLAs)* and *domain-specific languages (DSLs)* to design an extensible command-and-control simulator for Army fire support. The reusable components of our PLA are layers or "aspects" whose addition or removal simultaneously impacts the source code of multiple objects in multiple, distributed programs. The complexity of our component specifications is substantially reduced by using a DSL for defining and refining state machi ...

Keywords: GenVoca, aspects, domain-specific languages, refinements, simulation

4 Simulation sensitivity analysis using frequency domain experiments
D. J. Morrice, L. W. Schruben
October 1989 **Proceedings of the 21st conference on Winter simulation WSC '89**
Publisher: ACM Press

Full text available: pdf(561.85 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we review frequency domain experiments (FDE) for simulation sensitivity analysis and contrast it with conventional methodology. With very few runs of the model (often one or two runs is sufficient), FDE can be used to gain information on which factors significantly influence the performance of the simulated system. Two examples are given which illustrate some of the fundamental differences between frequency domain and conventional run-oriented analysis.

5 Special section: Reasoning about structure, behavior and function
B. Chandrasekaran, Rob Milne
July 1985 **ACM SIGART Bulletin**, Issue 93
Publisher: ACM Press
Full text available: pdf(5.13 MB) Additional Information: full citation, abstract, references, citings

The last several years' of work in the area of knowledge-based systems has resulted in a deeper understanding of the potentials of the current generation of ideas, but more importantly, also about their limitations and the need for research both in a broader framework as well as in new directions. The following ideas seem to us to be worthy of note in this connection.

6 The theory of parsing, translation, and compiling
Alfred V. Aho, Jeffrey D. Ullman
January 1972 Book
Publisher: Prentice-Hall, Inc.

Full text available: pdf(98.28 MB) Additional Information: full citation, abstract, references, citings, index terms

From volume 1 Preface (See Front Matter for full Preface)

This book is intended for a one or two semester course in compiling theory at the senior or graduate level. It is a theoretically oriented treatment of a practical subject. Our motivation for making it so is threefold.

(1) In an area as rapidly changing as Computer Science, sound pedagogy demands that courses emphasize ideas, rather than implementation details. It is our hope that the algorithms and concepts presen ...

7 I/O and scheduling: I/O processing in a virtualized platform: a simulation-driven approach

Vineet Chadha, Ramesh Illiikkal, Ravi Iyer, Jaideep Moses, Donald Newell, Renato J. Figueiredo

June 2007 **Proceedings of the 3rd international conference on Virtual execution environments VEE '07**

Publisher: ACM Press

Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references, index terms

Virtualization provides levels of execution isolation and service partition that are desirable in many usage scenarios, but its associated overheads are a major impediment for wide deployment of virtualized environments. While the virtualization cost depends heavily on workloads, it has been demonstrated that the overhead is much higher with I/O intensive workloads compared to those which are compute-intensive. Unfortunately, the architectural reasons behind the I/O performance overheads are ...

Keywords: performance model, simulation, virtual machines, virtualization, xen

8 A hierarchical multicast monitoring scheme

Joerg Walz, Brian Neil Levine

November 2000 **Proceedings of NGC 2000 on Networked group communication COMM '00**

Publisher: ACM Press

Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, index terms

Deployment of multicast routing services in corporate networks and Internet Service Providers is still tentative. Among other problems, there is a lack of monitoring and management tools and systems. Previous work in multicast management has failed to address the scalability problem present in multicast fault isolation and reporting. We propose a hierarchical, passive monitoring scheme, HPMM, that relies on a series of pre-deployed, self-organized monitoring daemons. With HPMM, fault message ...

9 Homeland security/emergency response: transportation security simulation: Detection of nuclear material at border crossings using motion correlation

David M. Nicol, Rose Tsang, Heidi Ammerlahn, Michael Johnson

December 2006 **Proceedings of the 38th conference on Winter simulation WSC '06**

Publisher: Winter Simulation Conference

Full text available: pdf(191.87 KB) Additional Information: full citation, abstract, references

This paper considers the problem that arises when a vehicle carrying nuclear material is detected approaching a border crossing. As quickly as possible, and with automation we wish to identify which vehicle among all those in the area is likely to be carrying the source. We show that if the border crossing area has technology for tracking the position of vehicles, we can correlate observed movements with observed changes in levels of detected radiation---for as the vehicle carrying the material ...

10 Level set and PDE methods for computer graphics

David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(17.07 MB) Additional Information: full citation, abstract, citings

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

11 New twists on memory management: Deconstructing process isolation

Mark Aiken, Manuel Fähndrich, Chris Hawblitzel, Galen Hunt, James Larus

October 2006 **Proceedings of the 2006 workshop on Memory system performance and correctness MSPC '06**

Publisher: ACM Press

Full text available: pdf(225.75 KB) Additional Information: full citation, abstract, references, index terms

Most operating systems enforce process isolation through hardware protection mechanisms such as memory segmentation, page mapping, and differentiated user and kernel instructions. Singularity is a new operating system that uses software mechanisms to enforce process isolation. A software isolated process (SIP) is a process whose boundaries are established by language safety rules and enforced by static type checking. SIPs provide a low cost isolation mechanism that provides failure isolation and ...

Keywords: hardware isolated process (HIP), hardware protection domain, singularity, software isolated process (SIP)

12 A scalable distributed information management system

Praveen Yalagandula, Mike Dahlin

August 2004 **ACM SIGCOMM Computer Communication Review , Proceedings of the 2004 conference on Applications, technologies, architectures, and protocols for computer communications SIGCOMM '04**, Volume 34 Issue 4

Publisher: ACM Press

Full text available: pdf(364.00 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a Scalable Distributed Information Management System (SDIMS) that *aggregates* information about large-scale networked systems and that can serve as a basic building block for a broad range of large-scale distributed applications by providing detailed views of nearby information and summary views of global information. To serve as a basic building block, a SDIMS should have four properties: scalability to many nodes and attributes, flexibility to accommodate a broad range of appl ...

Keywords: distributed hash tables, information management system, networked system monitoring

13 Modeling methodology for integrated simulation of embedded systems

Akos Ledeczi, James Davis, Sandeep Neema, Aditya Agrawal

January 2003 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 13 Issue 1

Publisher: ACM Press

Full text available: pdf(951.86 KB) Additional Information: full citation, abstract, references, citings, index terms

Developing a single embedded application involves a multitude of different development tools including several different simulators. Most tools use different abstractions, have their own formalisms to represent the system under development, utilize different input and output data formats, and have their own semantics. A unified environment that allows capturing the system in one place and one that drives all necessary simulators and

analysis tools from this shared representation needs a common r ...

Keywords: Simulation, domain specific languages, metamodeling, model integrated computing, modeling, simulation integration

14 Military applications: Security issues in high level architecture based distributed simulation

Asa Elkins, Jeffery W. Wilson, Denis Gracanin
December 2001 **Proceedings of the 33nd conference on Winter simulation WSC '01**
Publisher: IEEE Computer Society
Full text available: pdf(262.26 KB) Additional Information: full citation, abstract, references, index terms

The United States Department of Defense (DoD) has, over the past several years, emphasized the need to employ simulation based acquisition (SBA) in engineering and development. Distributed simulation introduces an information assurance challenge and details of a simulation must be guarded from unauthorized access. The High Level Architecture (HLA) and its Run-Time Interface (RTI) do not define support of mandatory access controls (MACs) or discretionary access controls (DACs) required to provide ...

15 Modeling methodology b: ontology driven simulation: An ontology for trajectory simulation

Umut Durak, Halit Oguztuzun, S. Kemal Ider
December 2006 **Proceedings of the 38th conference on Winter simulation WSC '06**
Publisher: Winter Simulation Conference
Full text available: pdf(646.15 KB) Additional Information: full citation, abstract, references

From the concept exploration for a weapon system to training simulators, from hardware-in-the-loop simulators to mission planning tools, trajectory simulations are used throughout the life cycle of a weapon system. A trajectory simulation can be defined as a computational tool to calculate the flight path and flight parameters of munitions. There is a wide span of trajectory simulations differing widely with respect to their performance and fidelity characteristics, from simple point-mass simula ...

16 Perfect Simulations for Random Trip Mobility Models

Santashil PalChaudhuri, Jean-Yves Le Boudec, Milan Vojnovic
April 2005 **Proceedings of the 38th annual Symposium on Simulation ANSS '05**
Publisher: IEEE Computer Society
Full text available: pdf(612.69 KB) Additional Information: full citation, abstract, citings, index terms

The random trip model was recently proposed as a generic mobility model that contains many particular mobility models, including the widely-known random waypoint and random walks, and accommodates more realistic scenarios. The probability distribution of the movement of a mobile in all these models typically varies with time and converges to a "steady state" distribution (viz. stationary distribution), whenever the last exists. Protocol performance during this transient phase and in steady-state ...

17 Simulation methods for RF integrated circuits

Ken Kundert
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design ICCAD '97**
Publisher: IEEE Computer Society
Full text available: pdf(97.56 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

The principles employed in the development of modern RF simulators are introduced and

the various techniques currently in use, or expected to be in use in the next few years, are surveyed. Frequency and time domain techniques are presented and contrasted, as are steady state and envelope techniques and large and small signal techniques.

Keywords: RF integrated circuits, envelope techniques, integrated circuit modelling, modern RF simulators, simulation methods, small signal techniques, state techniques, time domain techniques

18 CHARMS: a simple framework for adaptive simulation

Eitan Grinspun, Petr Krysl, Peter Schröder

July 2002 **ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual conference on Computer graphics and interactive techniques SIGGRAPH '02**, Volume 21 Issue 3

Publisher: ACM Press

Full text available: pdf(3.56 MB) Additional Information: full citation, abstract, references, citings, index terms

Finite element solvers are a basic component of simulation applications; they are common in computer graphics, engineering, and medical simulations. Although *adaptive* solvers can be of great value in reducing the often high computational cost of simulations they are not employed broadly. Indeed, building adaptive solvers can be a daunting task especially for 3D finite elements. In this paper we are introducing a new approach to produce *conforming, hierarchical, adaptive refinement meth ...*

***Keywords**: adaptive computation, basis function, multiresolution, refinement relation, subdivision*

19 Using abductive inferencing to derive complex error classifications for discrete sequential processes

Sanjeev B. Ahuja, James A. Reggia

March 1986 **Proceedings of the 19th annual symposium on Simulation ANSS '86**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.04 MB) Additional Information: full citation, references, index terms

20 Power grid and large interconnect network analysis: Large power grid analysis using domain decomposition

Quming Zhou, Kai Sun, Kartik Mohanram, Danny C. Sorensen

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(234.90 KB) Additional Information: full citation, abstract, references

This paper presents a domain decomposition (DD) technique for efficient simulation of large-scale linear circuits such as power distribution networks. Simulation results show that by integrating the proposed DD framework, existing linear circuit simulators can be extended to handle otherwise intractable systems.

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Computers & Chemical Engineering, Volume 20, Issues 6-7, June-July 1996, Pages 743-791
G. Stephanopoulos and C. Han
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☐	L2	(703/13,14,18.ccls. or 716/4,18.ccls.) and isolation logic	25
☐	L1	kapoor.in. and isolation logic	3

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